UHF Narrow band radio transceiver
STD-302 419MHz

Operation Guide

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GENERAL DESCRIPTION & FEATURES

General Description

The UHF FM narrow band semi-duplex radio data module STD-302 is a high performance transceiver designed for use in industrial applications requiring long range, high performance and reliability.

All high frequency circuits are enclosed inside a robust housing to provide superior resistance against shock and vibration. A narrow band technique enables high interference rejection and concurrent operation with multiple modules.

STD-302, a narrowband module with 25 kHz channel steps, achieves high TX/RX switching speed, making it an ideal RF unit for inclusion in feedback systems.

Features

- 10 mW RF power, 3.0 V operation
- Programmable RF channel
- Fast TX/RX switching time (5 ms)
- High sensitivity -119 dBm
- Excellent mechanical durability, high vibration & shock resistance

Applications

- Telemetry
  Water level monitor for rivers, dams, etc.
  Monitoring systems for environmental data such as temperature, humidity, etc.
  Transmission of measurement data (pressure, revolution, current, etc) to PC
  Security alarm monitoring
- Telecontrol
  Industrial remote control systems
  Remote control systems for factory automation machines
  Control of various driving motors
- Data transmission
  RS232/RS485 serial data transmission

SPECIFICATIONS

STD-302 419 MHz

All ratings at 25°C unless otherwise noted

Parameter	Rating	Conditions
General characteristics		
Communication method	Semi-duplex	
Oscillation type	PLL Controlled VCO	
Operating frequency range	418.725-419.425 MHz	
Channel step	Programmable	
Frequency stability	+/- 4 ppm	-10 to +55 °C
	+/- 8 ppm	-20 to +65 °C
Data rate	9600 bps max.	Input data pulse width: Min104μs, Max 5 ms
PLL reference frequency	21.25 MHz	
Operating temperature range	- 10 to + 55 °C	
	- 20 to + 65 °C	*A
Operating voltage range	3 - 5.5 V	
Dimensions	30 x 50 x 9 mm	
Transmitter part		
RF output power	9.0 mW	Antenna impedance 50 Ω
Deviation	2.5 kHz +/-0.35 kHz	PN9, 9600 bps, LPF 20 kHz
Deviation frequency characteristics	+/- 3 dB	50 - 4800 Hz
Residual FM noise	0.17 kHz	LPF 20 kHz
TX S/N	-30 dB	1 kHz, Dev.= +/-2.4 kHz CCITT filter
Spurious emission	-60 dBm	< 1 GHz
	-43 dBm	≥ 1 GHz
Adjacent channel leakage power	-37 dB	CH 25 kHz, BW 16 kHz, PN9, 9600 bps
Total distortion and noise	30 dB	1 kHz, Dev.+/-2.4 kHz, CCITT filter
Consumption current	40 mA	
Switching time RX to TX	5 - 10 ms	RX -> TX *1
Lock time	30 - 40 ms	Free Run -> TX *2
	10 - 20 ms	25 kHz channel shift *3
Receiver part		
Reception method	Double superheterodyne	
Sensitivity	-119 dBm (AF OUT)	1 kHz, Dev.+/-2.4 kHz, CCITT filter
Bit error rate	-110 dBm (Data Out)	9600 bps, PN9 (1/2556 bit error), Internal synchronous
AF output	150+/-35 mVrms	fmod.+/- 2.4 kHz, fm+/-1.2 kHz (RF level -30 dBm)
	140+/-35 mVrms	fmod.+/- 2.4 kHz, fm+/-2.4 kHz (RF level -30 dBm)
	120+/-45 mVrms	fmod.+/- 2.4kHz, fm+/-4.8 kHz (RF level -30 dBm)
RX S/N	35 dB	1 kHz, Dev.+/-2.4 kHz, CCITT filter (RF level -30 dBm)
Distortion	-30 dB	1 kHz, Dev.+/-2.4 kHz, CCITT filter (RF level -30 dBm)
Spurious emission	-60 dBm	
Spurious sensitivity	45 dB	Two signal method, Jamming signal = FM
Intermodulation	45 dB	Two signal method
Adjacent channel selectivity	45 dB	Two signal method, CH 25 kHz, Jamming signal = FM
Consumption current	26 mA	
Switching time TX to RX	5 - 10 ms	TX -> RX *1
Lock Time	30 - 40 ms	Free Run -> RX *2
	10 - 20 ms	25 kHz channel shift *3

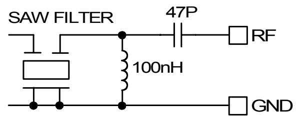
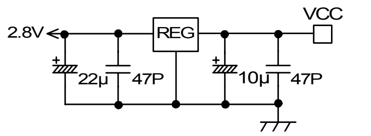
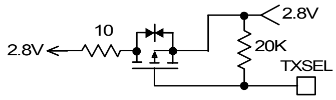
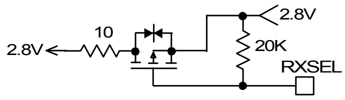
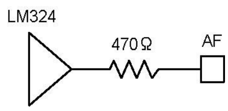
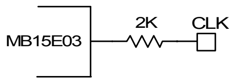
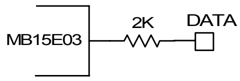
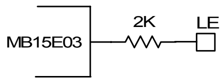
*A Under -10°C, the time required till effective data is output from DO is longer than that at normal temperature. It is recommended to use a preamble which is twice the length of the usual preamble. Please refer to page 12.

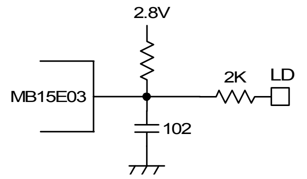
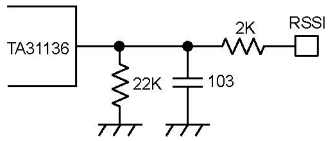
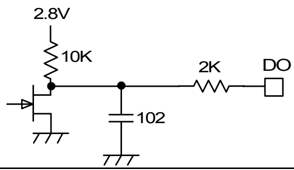
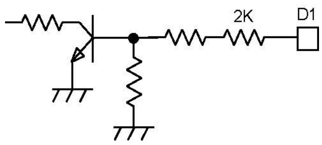
*1 Time required for the TX frequency or 1st local frequency to reach within +/-1.5 ppm of a stable frequency.

*2 Time required for the TX frequency or 1st local frequency to reach within +/-1.5 ppm of a stable frequency after PLL setting data is output.

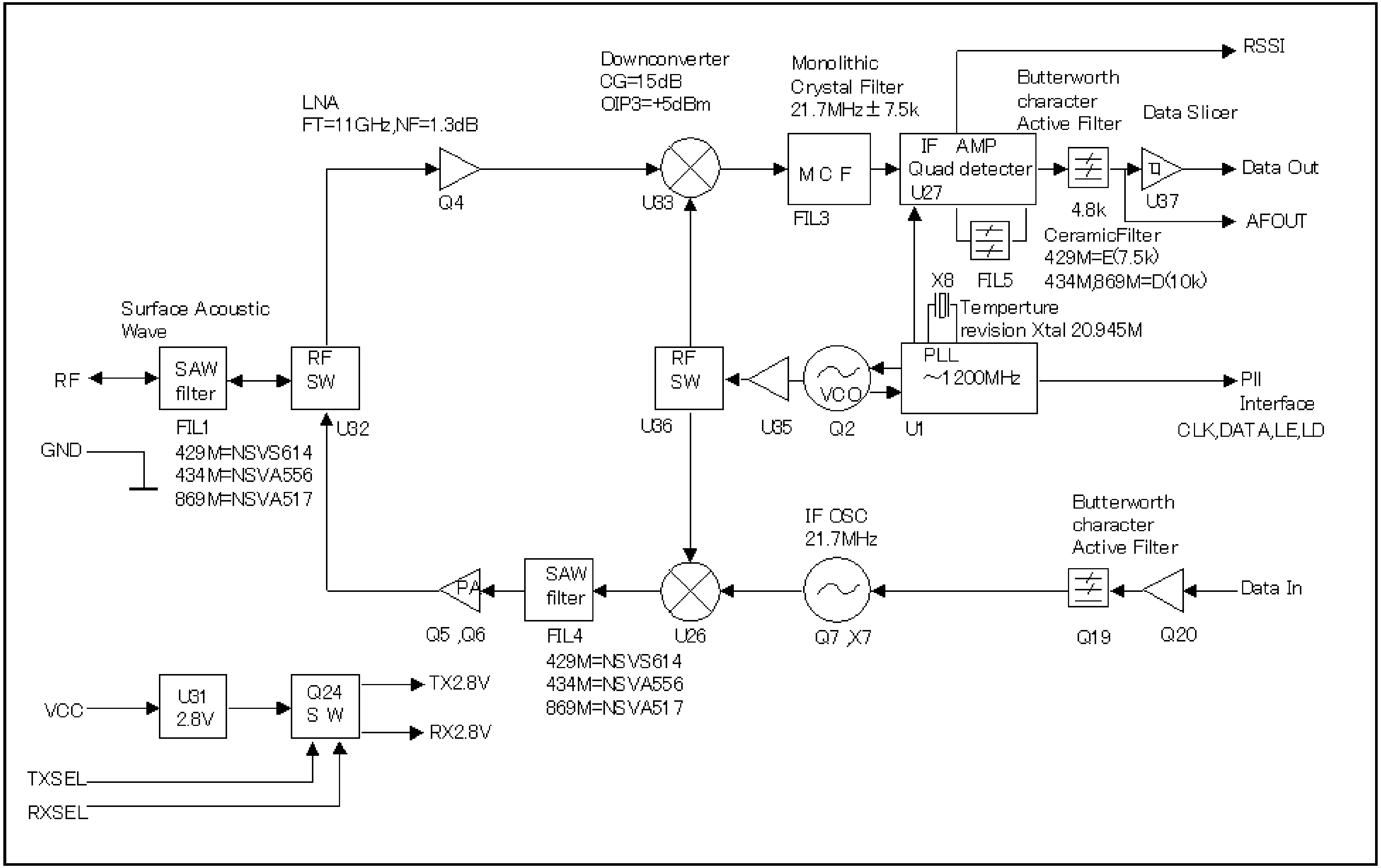
*3 Time required for the TX frequency or 1st local frequency to reach within +/-1.5 ppm of a stable frequency after PLL setting data for 25kHz shift is output.

PIN DESCRIPTION

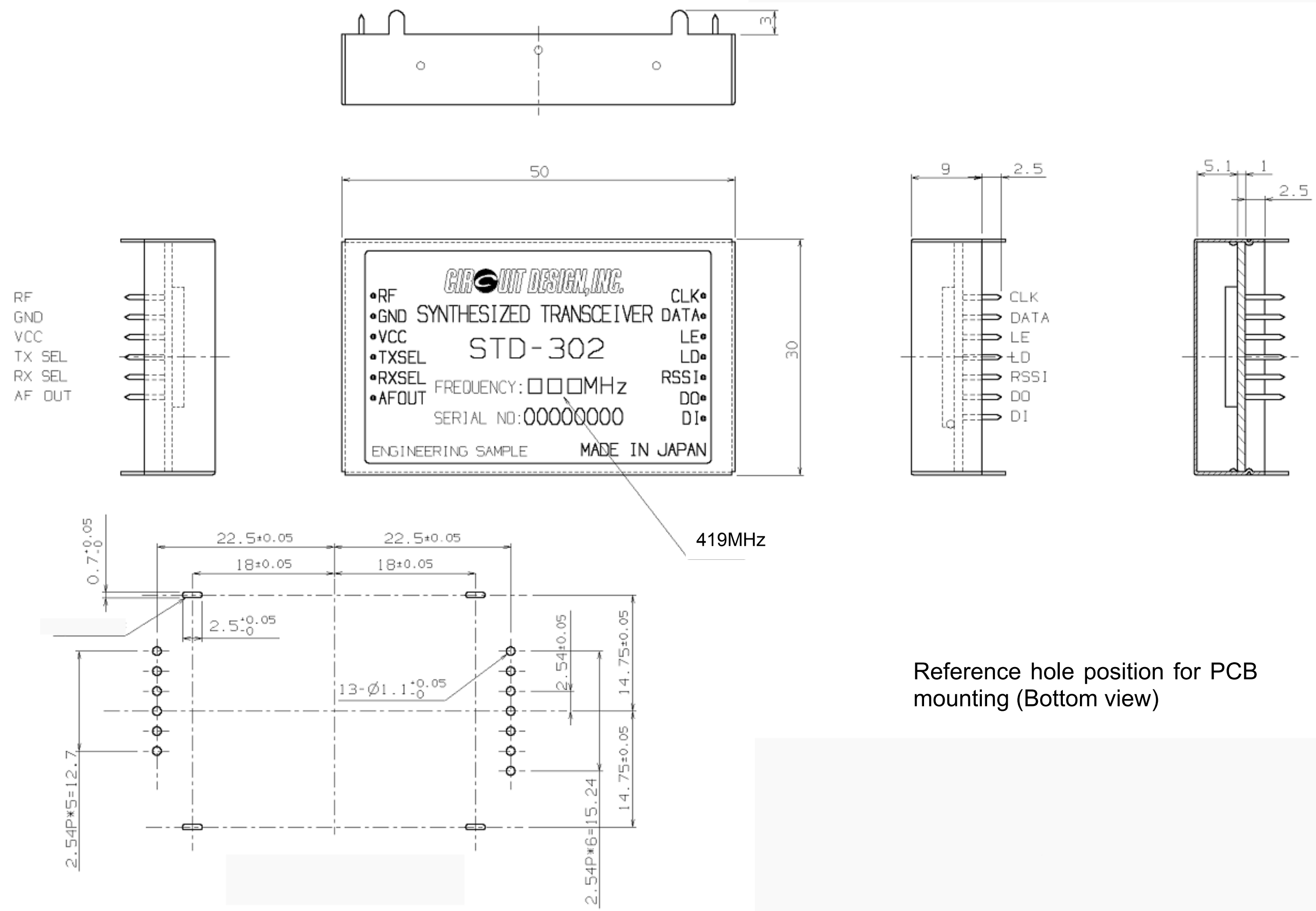
Pin name	I/O	Description	Equivalent circuit
RF	I/O	RF input terminal Antenna impedance nominal 50 **Ω**	
GND	I	GROUND terminal The GND pins and the feet of the shield case shoud be connected to the wide GND pattern.	
VCC	I	Power supply terminal DC 3.0 to 5.5 V	
TXSEL	I	TX select terminal GND = TXSEL active To enable the transmitter circuits, connect TXSEL to GND and RXSEL to OPEN or 2.8 V.	
RXSEL	I	RX select terminal GND= RXSEL active To enable the receiver circuits, connect RXSEL to GND and TXSEL to OPEN or 2.8 V.	
AF	I	Analogue output terminal There is DC offset of approx. 1 V. Refer to the specification table for amplitude level.	
CLK	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	
DATA	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	
LE	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	

LD	O	PLL lock/unlock monitor terminal Lock = H (2.8 V), Unlock = L (0 V)	
RSSI	O	Received Signal Strength Indicator terminal	
DO	O	Data output terminal Interface voltage: H=2.8V, L=0V	
DI	I	Data input terminal Interface voltage: H=Vcc, L=0V Input data pulse width Min.104 μs Max.5 ms	

BLOCK DIAGRAM <STD-302 419 MHz>



DIMENSIONS

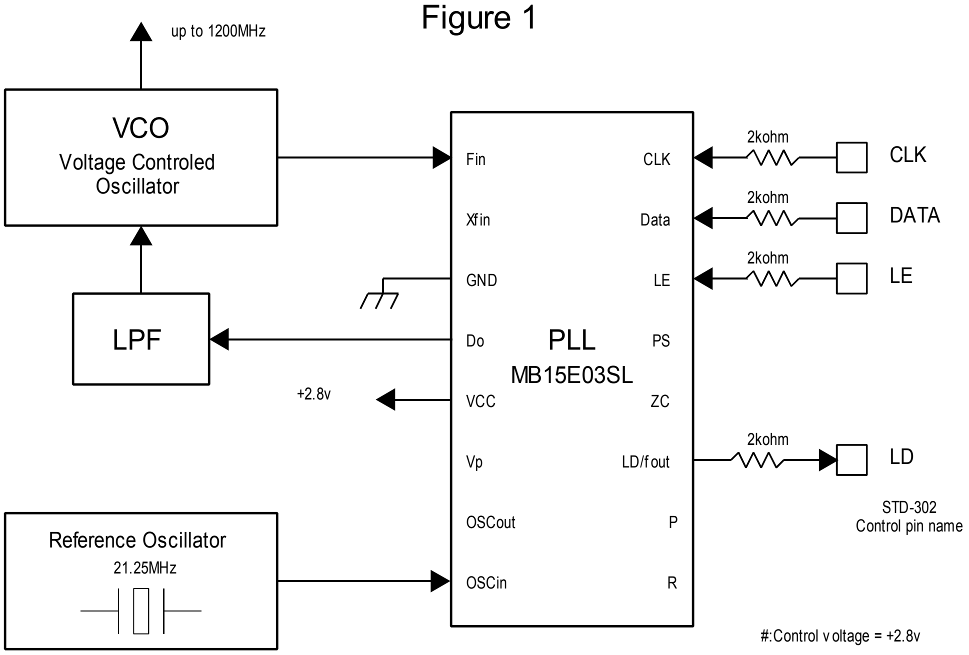


Reference hole position for PCB mounting (Bottom view)

PLL IC CONTROL

- **PLL IC control**

Figure 1



STD-302 is equipped with an internal PLL frequency synthesizer as shown in Figure 1. The operation of the PLL circuit enables the VCO to oscillate at a stable frequency. Transmission frequency is set externally by the controlling IC. STD-302 has control terminals (CLK, LE, DATA) for the PLL IC and the setting data is sent to the internal register serially via the data line. Also STD-302 has a Lock Detect (LD) terminal that shows the lock status of the frequency. These signal lines are connected directly to the PLL IC through a 2 kΩ resistor.

The interface voltage of STD-302 is 2.8 V, so the control voltage must be the same.
STD-302 comes equipped with a Fujitsu MB15E03SL PLL IC. Please refer to the manual of the PLL IC.

The following is a supplementary description related to operation with STD-302. In this description, the same names and terminology as in the PLL IC manual are used, so please read the manual beforehand.

- **How to calculate the setting values for the PLL register**

The PLL IC manual shows that the PLL frequency setting value is obtained with the following equation.
$f_{vco} = [(M \times N)+A] \times f_{osc} / R$ -- Equation 1
f_{vco} : Output frequency of external VCO
M: Preset divide ratio of the prescaler (64 or 128)
N: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$ A<N))
f_{osc}: Output frequency of the reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

With STD-302, there is an offset frequency (f_{offset}) 21.7 MHz for the transmission RF channel frequency f_{ch}. Therefore the expected value of the frequency generated at VCO (f_{expect}) is as below.
$f_{vco} = f_{expect} = f_{ch} - f_{offset}$ ---- Equation 2

The PLL internal circuit compares the phase to the oscillation frequency $f_{vco.}$ This phase comparison frequency (f_{comp}) must be decided. f_{comp} is made by dividing the frequency input to the PLL from the reference frequency oscillator by reference counter R. STD-302 uses 21.25 MHz for the reference clock $f_{osc.}$ f_{comp} is one of 6.25 kHz, 12.5 kHz or 25 kHz.

The above equation 1 results in the following with n = M x N + A, where “n” is the number for division.
$f_{vco}=n*f_{comp}$ ---- Equation 3 $n = f_{vco}/f_{comp}$ ---- Equation 4 note: $f_{comp} = f_{osc}/R$

Also, this PLL IC operates with the following R, N, A and M relational expressions.
$R=f_{osc}/f_{comp}$ ---- Equation 5 N = INT (n / M) ---- Equation 6 A = n - (M x N) ---- Equation 7
INT: integer portion of a division.

As an example, the setting value of RF channel frequency f_{ch} 869.725 MHz can be calculated as below.
The constant values depend on the electronic circuits of STD-302.

Conditions:	Channel center frequency:	f_{ch} = 869.725 MHz
	Constant: Offset frequency:	f_{offset}=21.7 MHz
	Constant: Reference frequency:	f_{osc}=21.25 MHz
	Set 25 kHz for Phase comparison frequency and 64 for Prescaler value M	

The frequency of VCO will be
$f_{vco} = f_{expect} = f_{ch} - f_{offset}$ = 869.725 –21.7 = 848.025MHz
Dividing value “n” is derived from Equation 4
$n = f_{vco} / f_{comp}$ = 848.025MHz/25kHz = 33921
Value “R” of the reference counter is derived from Equation 5.
$R = f_{osc}/f_{comp}$ = 21.25MHz/25kHz = 850
Value “N” of the programmable counter is derived from Equation 6.
N = INT (n/M) = INT(33921/64) = 530
Value “A“ of the swallow counter is derived from Equation 7.
A = n – (M x N) = 33921 – 64 x 530 = 1

The frequency of STD-302 is locked at a center frequency f_{ch} by inputting the PLL setting values N, A and R obtained with the above equations as serial data. The above calculations are the same for the other frequencies.
Excel sheets that contain automatic calculations for the above equations can be found on our web site (www.circuitdesign.jp/eng/).

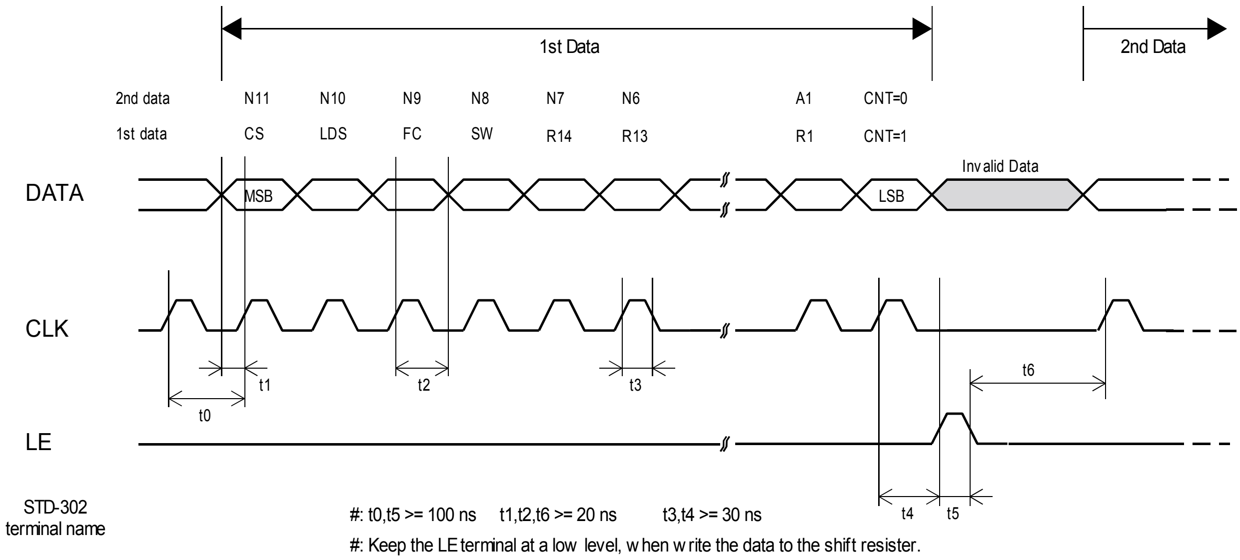
The result of the calculations is arranged as a table in the CPU ROM. The table is read by the channel change routine each time the channel is changed, and the data is sent to the PLL.

- **Method of serial data input to the PLL**

After the RF channel table plan is decided, the data needs to be allocated to the ROM table and read from there or calculated with the software.
Together with this setting data, operation bits that decide operation of the PLL must be sent to the PLL.
The operation bits for setting the PLL are as follows. These values are placed at the head of the reference counter value and are sent to the PLL.

1. CS: Charge pump current select bit
   CS = 0 +/-1.5 mA select VCO is optimized to +/-1.5 mA
2. LDS: LD/fout output setting bit
   LDS = 0 LD select Hardware is set to LD output
3. FC: Phase control bit for the phase comparator
   FC = 1 Hardware operates at this phase

Figure 2



The PLL IC, which operates as shown in the block diagram in the manual, shifts the data to the 19-bit shift register and then transfers it to the respective latch (counter, register) by judging the CNT control bit value input at the end.

1. CLK [Clock]: Data is shifted into the shift register on the rising edge of this clock.
2. LE [Load Enable]: Data in the 19-bit shift register is transferred to respective latches on the rising edge of the clock. The data is transferred to a latch according to the control bit CNT value.
3. Data [Serial Data]: You can perform either reference counter setup or programmable counter setup first.

TIMING CHART

Control timing in a typical application is shown in Figure 3.
Initial setting of the port connected to the radio module is performed when power is supplied by the CPU and reset is completed. MOS-FET for supply voltage control of the radio module, RXSEL and TXSEL are set to inactive to avoid unwanted emissions. The power supply of the radio module is then turned on. When the radio module is turned on, the PLL internal resistor is not yet set and the peripheral VCO circuit is unstable. Therefore data transmission and reception is possible 40 ms after the setting data is sent to the PLL at the first change of channel, however from the second change of channel, the circuit stabilizes within 20 ms and is able to handle the data.
Changing channels must be carried out in the receive mode. If switching is performed in transmission mode, unwanted emission occurs.

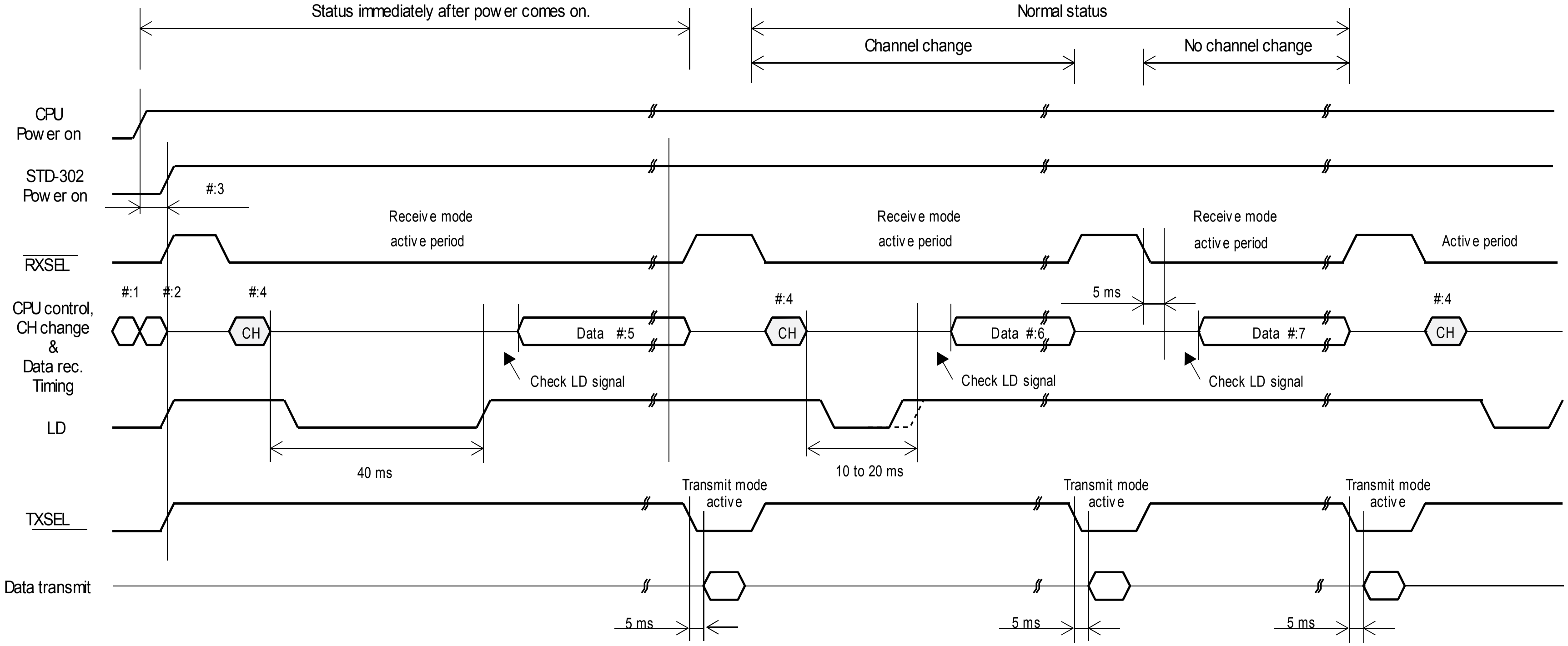
If the module is switched to the receive mode when operating in the same channel, (a new PLL setting is not necessary) it can receive data within 5 ms of switching[*1]. For data transmission, if the RF channel to be used for transmission is set while still in receiving mode, data can be sent at 5 ms after the radio module is switched from reception to transmission[*2].
Check that the Lock Detect signal is “high” 20 ms after the channel is changed. In some cases the Lock Detect signal becomes unstable before the lock is correctly detected, so it is necessary to note if processing of the signal is interrupted. It is recommended to observe the actual waveform before writing the process program.

[*1] DC offset may occur due to frequency drift caused by ambient temperature change. Under conditions below -10 °C, 10 to 20 ms delay of DO output is estimated. The customer is urged to verify operation at low temperature and optimize the timing.

[*2] Sending ‘10101…..’ preamble just after switching to transmission mode enables smoother operation of the binarization circuit of the receiver.
For 9600 bps, a preamble of ‘11001100’ is effective.
Recommended preamble length:
-10 °C - +55°C: 15 ms
-20 °C - +65 °C (for operation exceeding the above range): 30 ms

Remark
For details about PLL control and the sample programs, see our technical document ‘STD-302 interface method’

Figure 3: Timing diagram for STD-302



#:1 Reset control CPU

#:2 Initialize the port connected to the module.

#:3 Supply power to the module after initializing CPU.

#:4 RFchannel change must be performed in receiving mode.

#:5 40 ms later, the receiver can receive the data after changing the channel..

#:6 10 to 20 ms later, the receiver can receive the data after changing the channel.

#:7 5 ms later, the data can be received if the RF channel is not changed.

PLL FREQUENCY SETTING DATA REFERENCE

419 MHz ISM band (418.725 – 419.425 MHz)

Parameter name	Value
Phase Comparing Frequency F_{comp} [kHz]	25
Start Channel Frequency F_{ch} [MHz]	418.7250
Channel Step Frequency [kHz]	25
Number of Channel	29
Prescaler M	64

(green)	: For data input
(yellow)	: Result of calculation
(light blue)	: Fixed value

Parameter name	Value
Reference Frequency F_{osc} [MHz]	21.25
Offset Frequency F_{offset} [MHz]	21.7

Parameter name	Value
Reference Counter R	850
Programmable Counter N Min. Value	248
Programmable Counter N Max. Value	248
Swallow Counter A Min. Value	9
Swallow Counter A Max. Value	37

No.	Channel Frequency FCH (MHz)	Expect Frequency FEXPECT (MHz)	Lock Frequency FVCO (MHz)	Number of Division n	Programmable Counter N	Swallow Counter A
0	418.7250	397.0250	397.0250	15881	248	9
1	418.7500	397.0500	397.0500	15882	248	10
2	418.7750	397.0750	397.0750	15883	248	11
3	418.8000	397.1000	397.1000	15884	248	12
4	418.8250	397.1250	397.1250	15885	248	13
5	418.8500	397.1500	397.1500	15886	248	14
6	418.8750	397.1750	397.1750	15887	248	15
7	418.9000	397.2000	397.2000	15888	248	16
8	418.9250	397.2250	397.2250	15889	248	17
9	418.9500	397.2500	397.2500	15890	248	18
10	418.9750	397.2750	397.2750	15891	248	19
11	419.0000	397.3000	397.3000	15892	248	20
12	419.0250	397.3250	397.3250	15893	248	21
13	419.0500	397.3500	397.3500	15894	248	22
14	419.0750	397.3750	397.3750	15895	248	23
15	419.1000	397.4000	397.4000	15896	248	24
16	419.1250	397.4250	397.4250	15897	248	25
17	419.1500	397.4500	397.4500	15898	248	26
18	419.1750	397.4750	397.4750	15899	248	27
19	419.2000	397.5000	397.5000	15900	248	28
20	419.2250	397.5250	397.5250	15901	248	29
21	419.2500	397.5500	397.5500	15902	248	30
22	419.2750	397.5750	397.5750	15903	248	31
23	419.3000	397.6000	397.6000	15904	248	32
24	419.3250	397.6250	397.6250	15905	248	33
25	419.3500	397.6500	397.6500	15906	248	34
26	419.3750	397.6750	397.6750	15907	248	35
27	419.4000	397.7000	397.7000	15908	248	36
28	419.4250	397.7250	397.7250	15909	248	37

Regulatory compliance information

Compliance

STD-302 419 MHz was designed to be installed in radio equipment for use in China. The regulations and the technical specifications referred to in the design phase are shown in Table 1 and 2 below.

Table 1 Regulation

Product	STD-302 419 MHz
Country	China
Application specified	419 MHz band for industrial remote control device
Generic regulation	Preliminary regulation for low power (short range) devices (Ministry of Information Industry May 1998)
Reference URL	SRRC: http://www.srrc.gov.cn/

Table 2 Specification

Specification specified in the generic regulation	
Frequency	418.950 MHz, 418.975 MHz, 419.000 MHz, 419.025 MHz, 419.050 MHz, 419.075 MHz, 419.100 MHz, 419.125 MHz, 419.150 MHz, 419.175 MHz, 419.200 MHz, 419.250 MHz, 419.275MHz
Output power	≤ 10 mW
Band width	≤ 16 kHz
Spurious emission	≤ 2.5 μW
Frequency tolerance	$\leq 4 \times 10^{-6}$

The relevant laws and regulations are subject to change. Circuit Design, Inc. is not responsible for the validity and the accuracy of our understanding and translation relating to the regulation and specification above.

Compliance assessment

This product was designed to meet the specification above, however it has not been assessed for conformity with the appropriate regulations. Uses are required to verify that their final product meets the appropriate specifications and to perform the procedures for regulatory compliance.

Guarantee of regulatory compliance

We only guarantee that this product meets the specification in this document. We are exempt from any other responsibilities relating to regulatory compliance.

We also recommend that the user consults the authorities in the relevant country for detailed regulatory information such as valid regulations, test specifications, assessment procedures, marking methods etc, before starting any project with this product.
If technical documentation is required for compliance assessments, we will provide any documents, which may be considered necessary for assessment, under NDA. The documentation is only available in English.

Cautions

- As the radio module communicates using electronic radio waves, there are cases where transmission will be temporarily cut off due to the surrounding environment and method of usage. The manufacturer is exempt from all responsibility relating to resulting harm to personnel or equipment and other secondary damage.
- Do not use the equipment within the vicinity of devices that may malfunction as a result of electronic radio waves from the radio module.
- The manufacturer is exempt from all responsibility relating to secondary damage resulting from the operation, performance and reliability of equipment connected to the radio module.
- Communication performance will be affected by the surrounding environment, so communication tests should be carried out before actual use.
- Ensure that the power supply for the radio module is within the specified rating. Short circuits and reverse connections may result in overheating and damage and must be avoided at all costs.
- Ensure that the power supply has been switched off before attempting any wiring work.
- The case is connected to the GND terminal of the internal circuit, so do not make contact between the '+' side of the power supply terminal and the case.
- When batteries are used as the power source, avoid short circuits, recharging, dismantling, and pressure. Failure to observe this caution may result in the outbreak of fire, overheating and damage to the equipment. Remove the batteries when the equipment is not to be used for a long period of time. Failure to observe this caution may result in battery leaks and damage to the equipment.
- Do not use this equipment in vehicles with the windows closed, in locations where it is subject to direct sunlight, or in locations with extremely high humidity.
- The radio module is neither waterproof nor splash proof. Ensure that it is not splashed with soot or water. Do not use the equipment if water or other foreign matter has entered the case.
- Do not drop the radio module or otherwise subject it to strong shocks.
- Do not subject the equipment to condensation (including moving it from cold locations to locations with a significant increase in temperature.)
- Do not use the equipment in locations where it is likely to be affected by acid, alkalis, organic agents or corrosive gas.
- Do not bend or break the antenna. Metallic objects placed in the vicinity of the antenna will have a great effect on communication performance. As far as possible, ensure that the equipment is placed well away from metallic objects.
- The GND for the radio module will also affect communication performance. If possible, ensure that the case GND and the circuit GND are connected to a large GND pattern.

Warnings

- Do not take a part or modify the equipment.
- Do not remove the product label (the label attached to the upper surface of the module.) Using a module from which the label has been removed is prohibited.