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BR88

SRD	AUDIO RX	860-870 MHz

860-870 MHz AUDIO PLL RECEIVER MODULE WITH PILOT TONE DECODER (RDS)

BR88V3	3 Vcc audio Rx module (3 V logic interface)
BR88V5	5 Vcc audio Rx module (5 V logic interface)

Frequency	…….	860-870 MHz (1)
Sensitivity	…….	-100 dBm (20 dB SINAD) (1 kHz dev. 10 kHz)
Selectivity	…….	± 140 kHz
Modulation	…….	FM (dev. ± 30 kHz max.)
Audio output level	……..	30 mV_{RMS} (100 mVpp - 100kΩ load)
Audio response	……..	100 – 8000 Hz
RDS data output	……..	200 Baud max.

Note (1) : 863-865 MHz audio wireless band CEPT ERC REC 70-03 annex 13

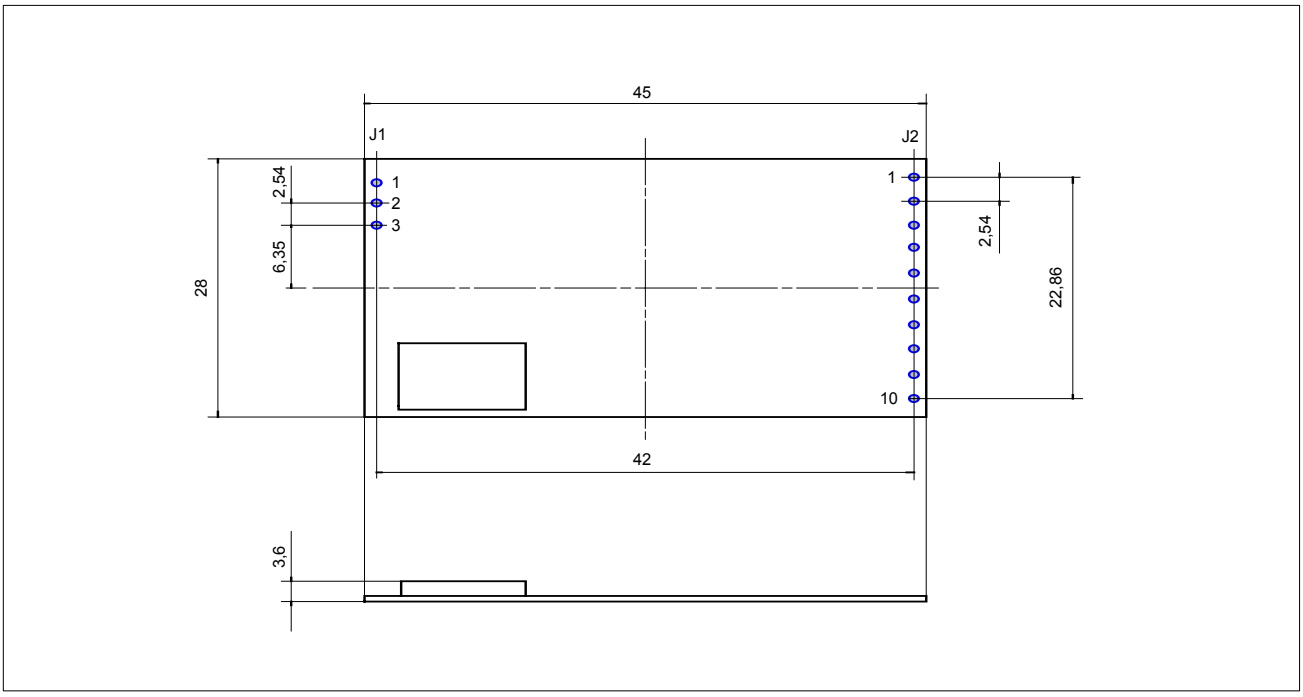

Fig.1 Phisical dimensions

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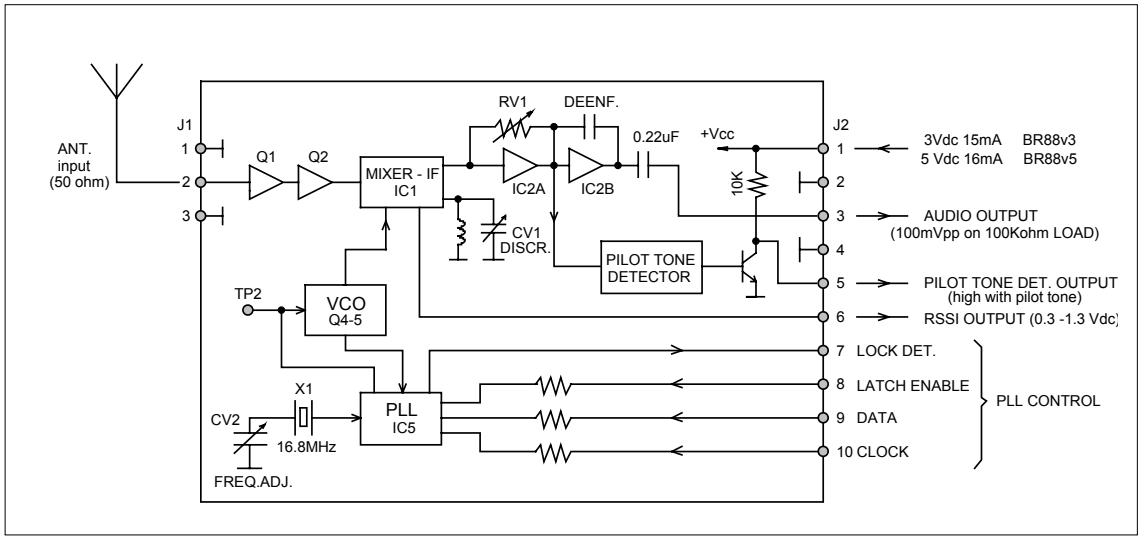

Fig.2 Functional block diagram

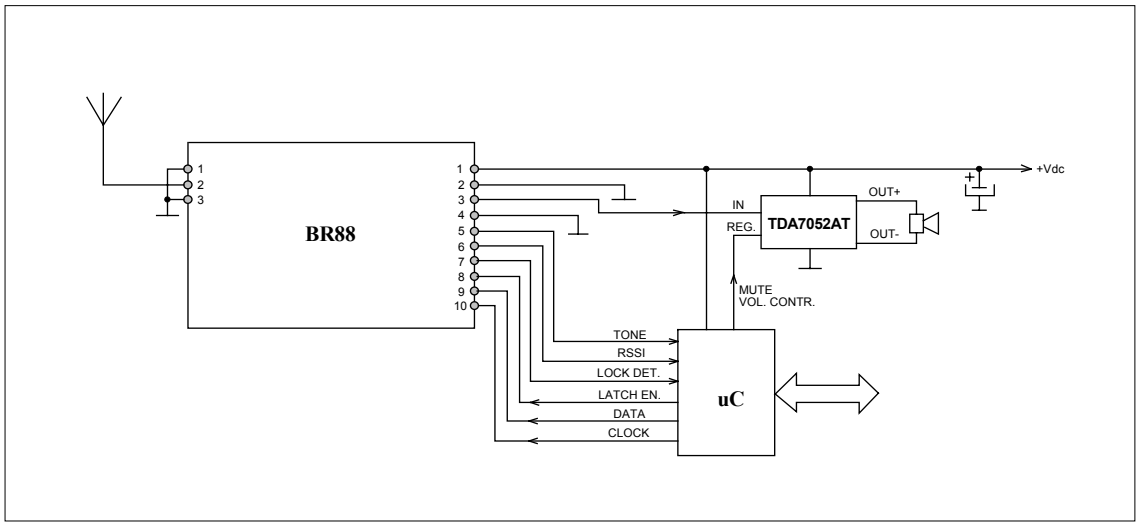

Fig. 3 BR88 receiver electrical connections

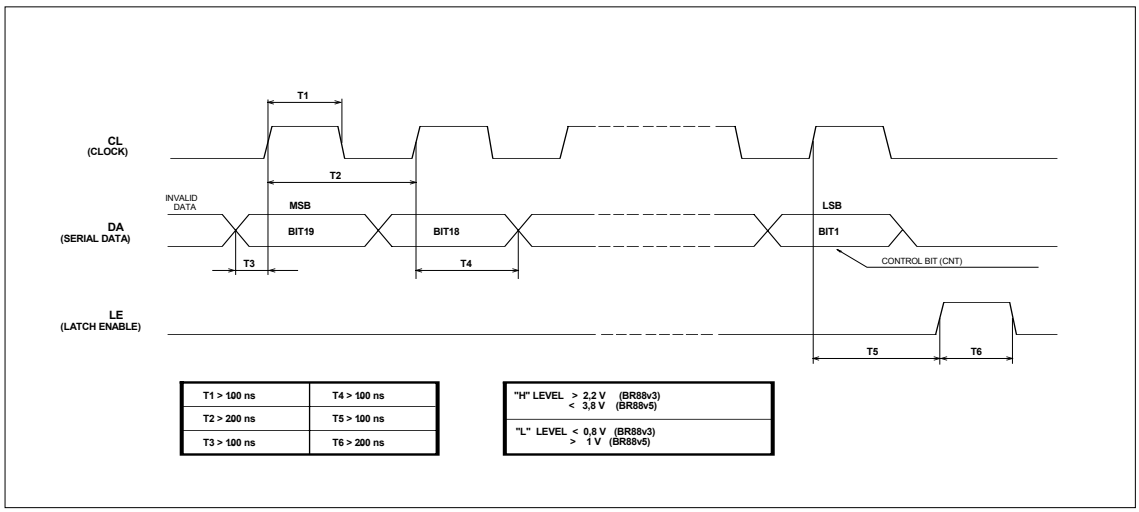

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Fig. 4 - Serial interface timing diagram.

FREQUENCY PROGRAMMING

1) The "PLL" frequency synthesizer

Receiver local oscillator frequency is generated by a low phase-noise "VCO" (Voltage Controlled Oscillator) locked by a "PLL" circuit (Fujitsu MB15E03SL) to the reference 16.800 MHz Xtal (X1 in fig.2).

2) Serial control interface description

A 3 wires serial control interface (clock, data and latch enable) is used to program the "PLL" IC (fig.2). Data are written into the 19-bit shift register (see fig.5) at the rising edge of the "CL" (clock) signal (MSB first).
Data are then transferred into the appropriate 18-bit latch at the rising edge of the "LE" (latch enable) pulse depending on the "CNT" (control bit) value.
"R" latch is loaded if "CNT" bit is set to "1", "N" latch is loaded with "CNT" = 0.
To program a frequency two 19-bit long words must be written into the shift register : the "R" word and the "N" word.

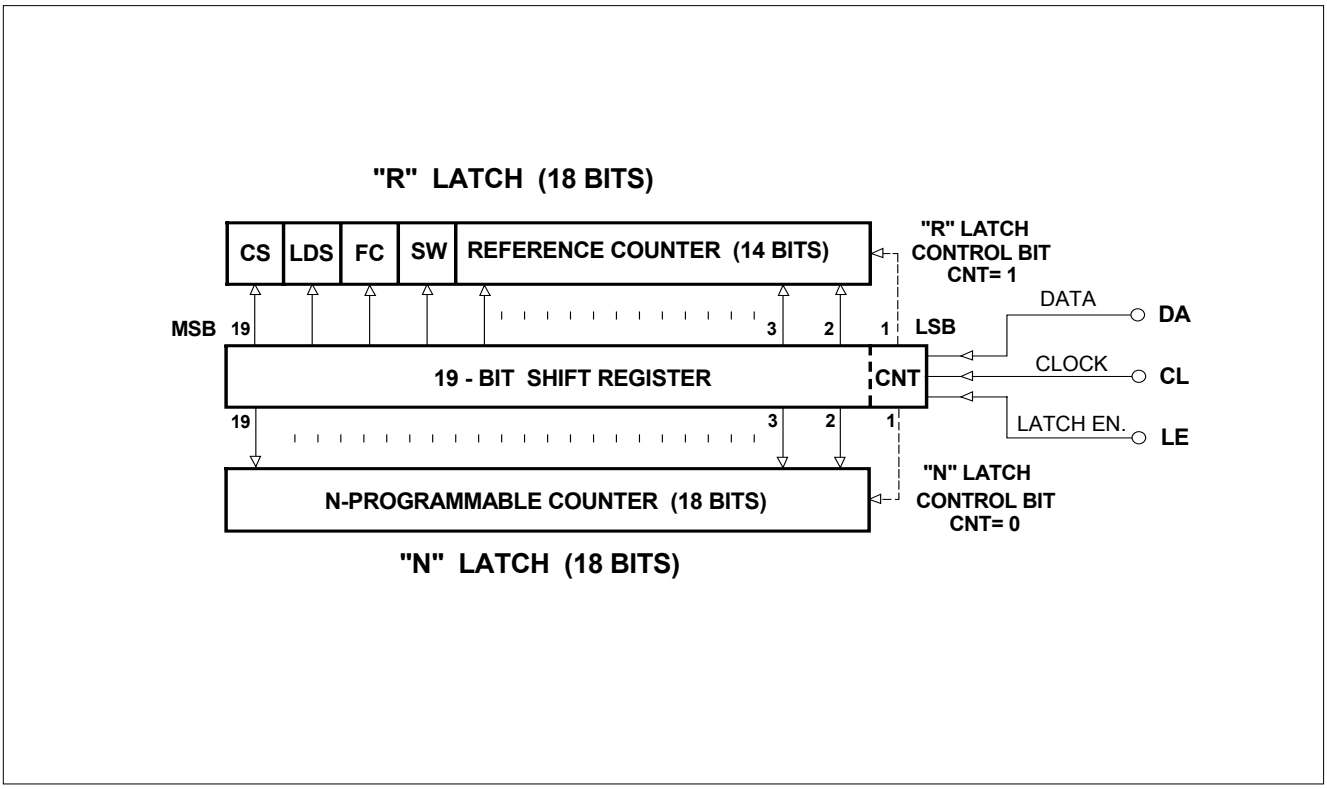

Fig. 5 - PLL internal register and latches.

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3) PLL frequency synthesizer parameters

PLL IC	: Fujitsu MB15E03SL
Reference frequency	: 16.800 MHz
Programming frequency step	: 50 kHz
"SW" bit (bit 16 of "R" word) = 1	: prescaler divide ratio = 64/65
"FC" bit (bit 17 of "R" word) = 1	: phase comparator positive output
"LDS" bit (bit 18 of "R" word) = 0	: lock-detect signal available
"CS" bit (bit 19 of "R" word) = 1	: charge – pump current = 6 mA

Note : *Although these are the reccomended parameters, different "PLL" programming modes can be implemented, if necessary . Refer to MB15E03SL data sheet at www.fujitsumicro.com for further informations.*

4) R - word

Bit 1 (CNT) must be set to "1".
Bits from 2 to 15 are the "R" number
Bits from 16 to 19 are the "SW", "FC", "LDS" and "CS" bits.

"R" is the value that is preset into the PLL reference divider and is calculated dividing the reference frequency (16800 kHz) by the required minimum programming frequency step.

For a 50 kHz frequency step :

$$R = 16800 / 50 = 336 \qquad (150H)$$

R word - example

Frequency step = 50 kHz ("R" = 150H)
"CS" = 1 (PLL charge – pump current = 6 mA)

"R" word

MSB ← SHIFT LSB

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**
CS	LDS	FC	SW	R														CNT

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5) N-word

Bit 1 (CNT) must be "0".

Bits from 2 to 19 are the "N" number.

"N" value is calculated dividing the receive required frequency minus 10700 kHz (the IF frequency) by the frequency step.

NOTE: Due to the internal architecture of the "PLL" IC , when "SW" bit of R-WORD (bit n. 16) is "1" (prescaler divide ratio = 64/65), bit n. 8 of N-word must not be used . It must be fixed to "0" and ignored.

N word - example

Receiver frequency = 863.250 MHz
"N" = 863250-10700 / 50 = 17051 (429BH)

"N" word

MSB ← SHIFT (*) LSB

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**0**

N CNT

Note (*) : Bit n.8 is fixed to "0" and ignored.

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Lock detect output (LD –J2 pin n. 7)

During normal operation, the " PLL" is locked to the correct programmed frequency and the LD output is high (+3 V).

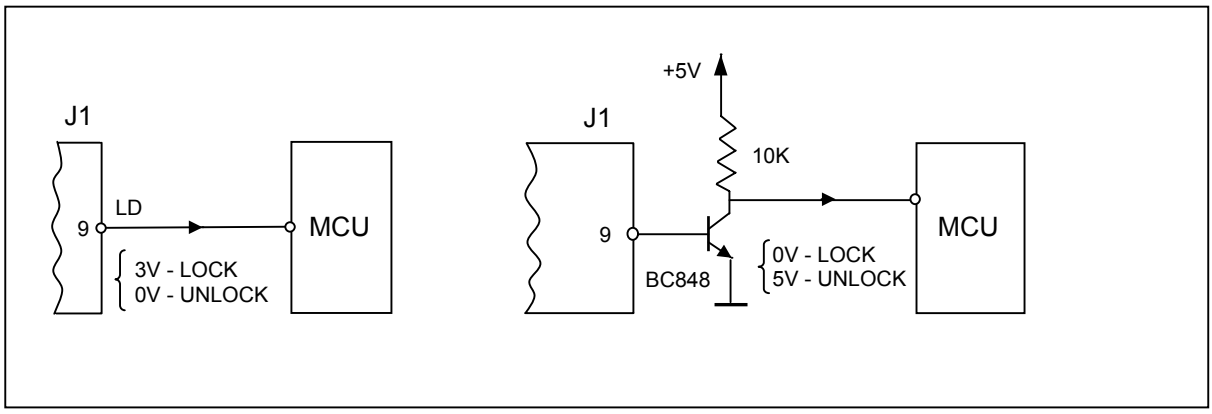

Fig. 6 Lock detect output interface to MCU.

During normal operation, it is not usually necessary to control the "UNLOCK" situation.
An "UNLOCK" situation is possible during a long period of continuos reception : in this case the MCU detects the "UNLOCK" state and provides to resend the appropriate programming words.

Note : Avoid to sample the "LD" status immediately after the programming sequence. A time of 100 ms or more , also between subsequent "LD" controls , is recommended.

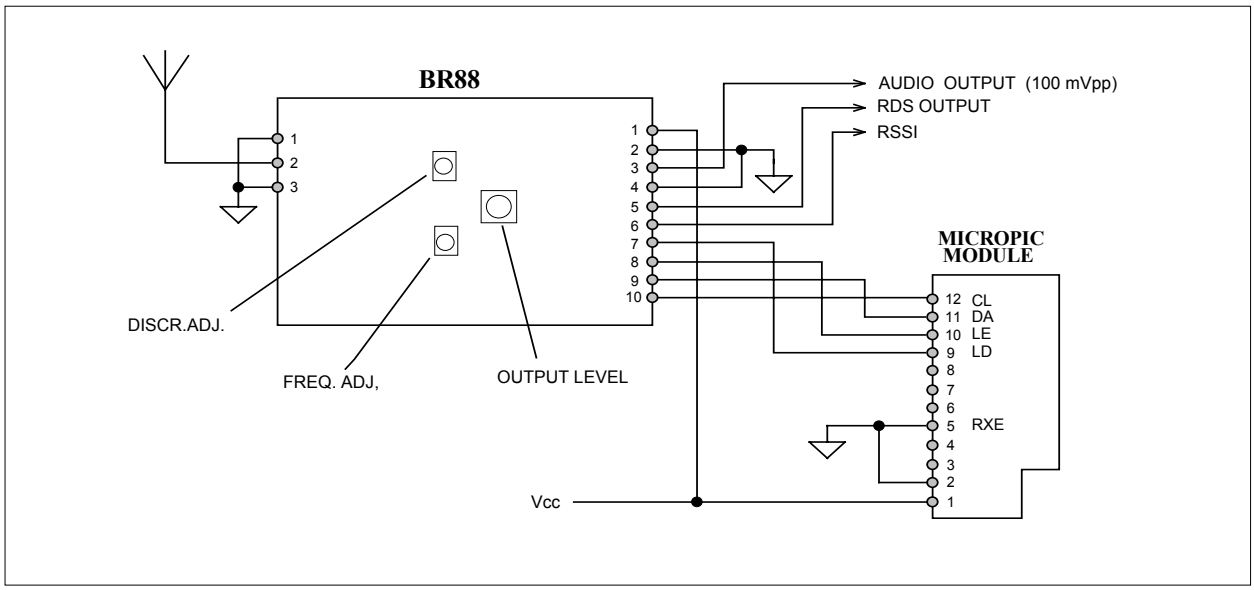

Fig. 7 - BR88 receiver test setup with frequency programming from micropic module.